**Improved Balancing And Sensing of Sub-module Capacitor Voltages In Modular Multi-level Converters Implementation Using Verilog HDL**

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| Group Members:- | Paaban Panda | 22115110 |
|  | Lakshay Data | 22117072 |
|  | Dhruv Sagar | 22115051 |

Branch:- Electrical Engineering

Year- II

**AIM:-**

To sort the capacitor in order of their voltage and to determine which capacitor to remain ON and which capacitor to be bypassed based the capacitor voltage and the requirement of number of capacitors to remained ON.

Here is the implementation of a 7- level three phase MMC. So there will be 6 capacitors in both upper and lower arms.

Here the input voltages of all capacitors and the current value are floating point values that are represented according to 32-bit single precision IEEE 754 convention.

**Component Modules Used**

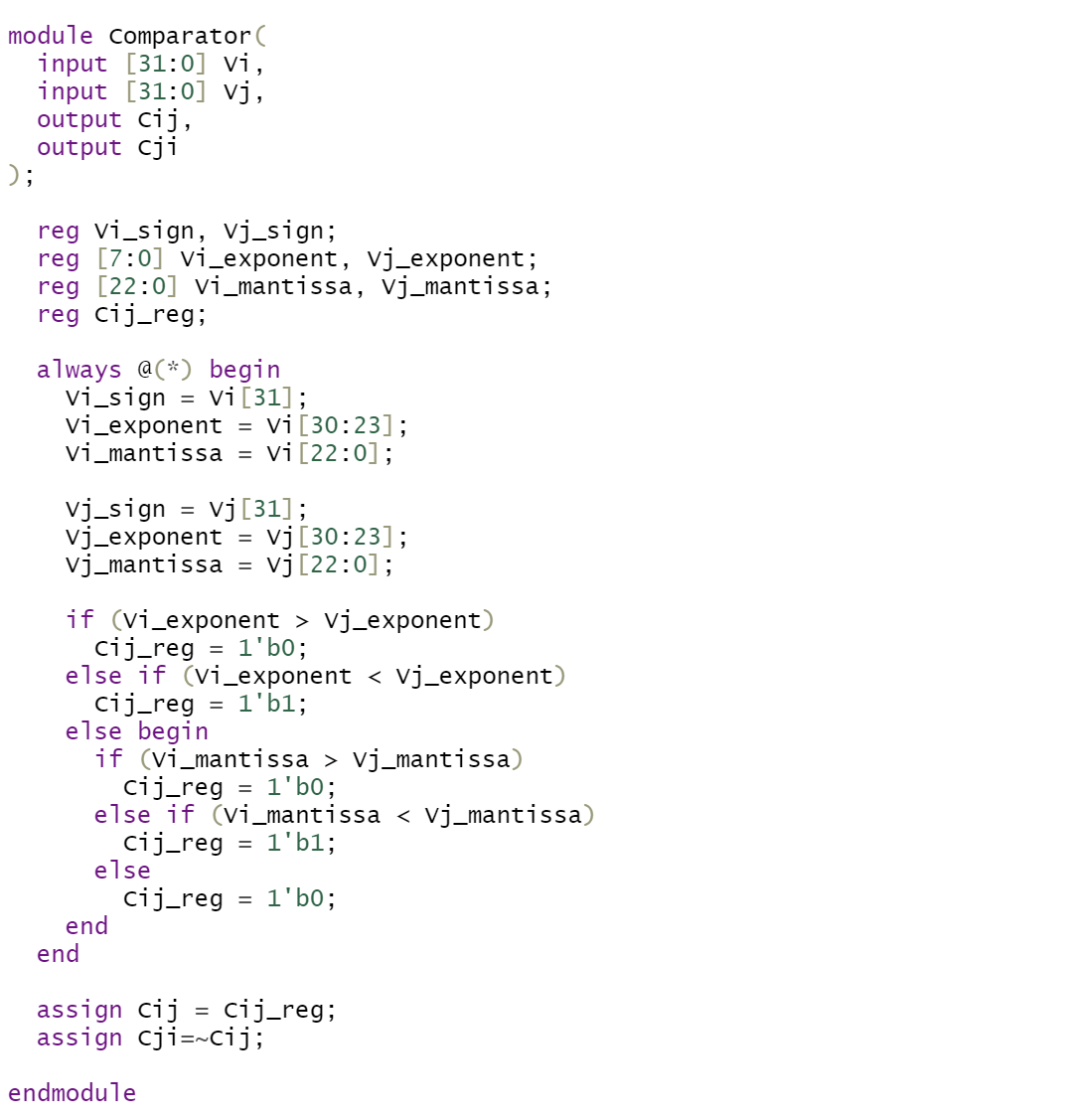
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| **SL. NO.** | **Module Name** | **Functionality** |
| **1** | **Comparator** | **To determine if CiCj is logic high or low based in values of Vi and Vj.** |
| **2** | **LogicalORCombination** | **To find the logic OR of all possible combination of ‘r’ numbers AND together.** |

1. Comparator

Input:- Vi and Vj.

Output:- Cij and Cji.

Based on relative values of Vi and Vj it decides the value of Cij and Cji  to be logic high or logic low.

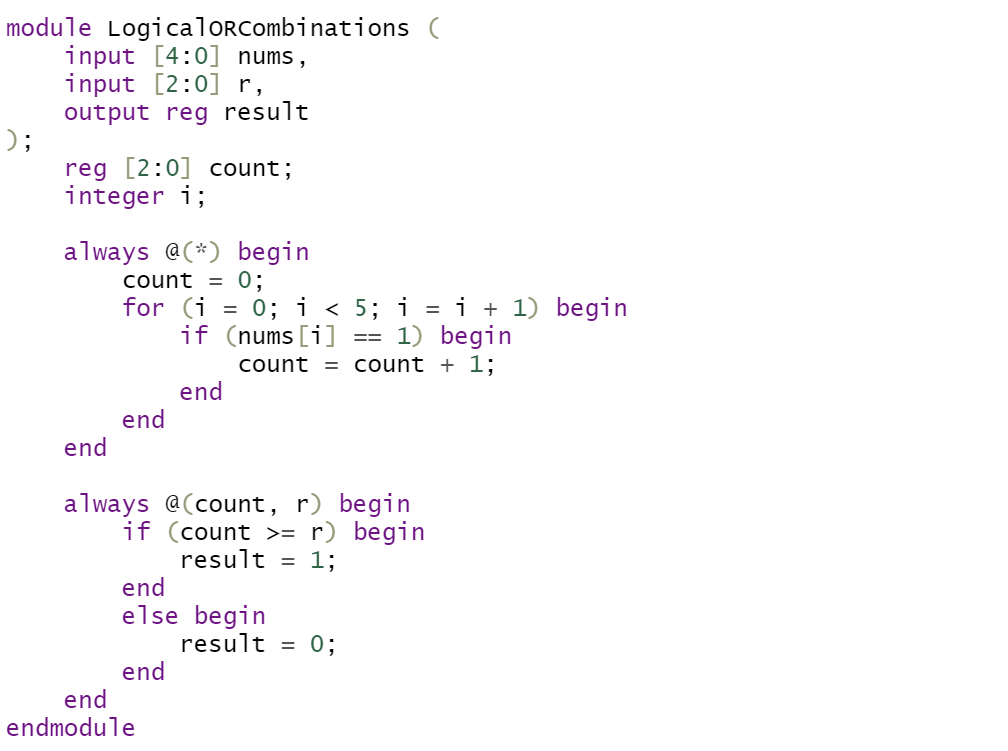


1. **LogicalORCombination**

Input:- num(5 bit binary), r(3-bit binary).

Output:- result.

num is array of length 5 out which r numbers are to chosen at a time and all the chosen r numbers needs to be logically AND and the logical AND of all the combinations needs to be ORed and output to be returned as result.



**Top Level Module**

Input:- Voltages of all 12 capacitors, Input current(I), n.

Output:-M(12 bit binary number).

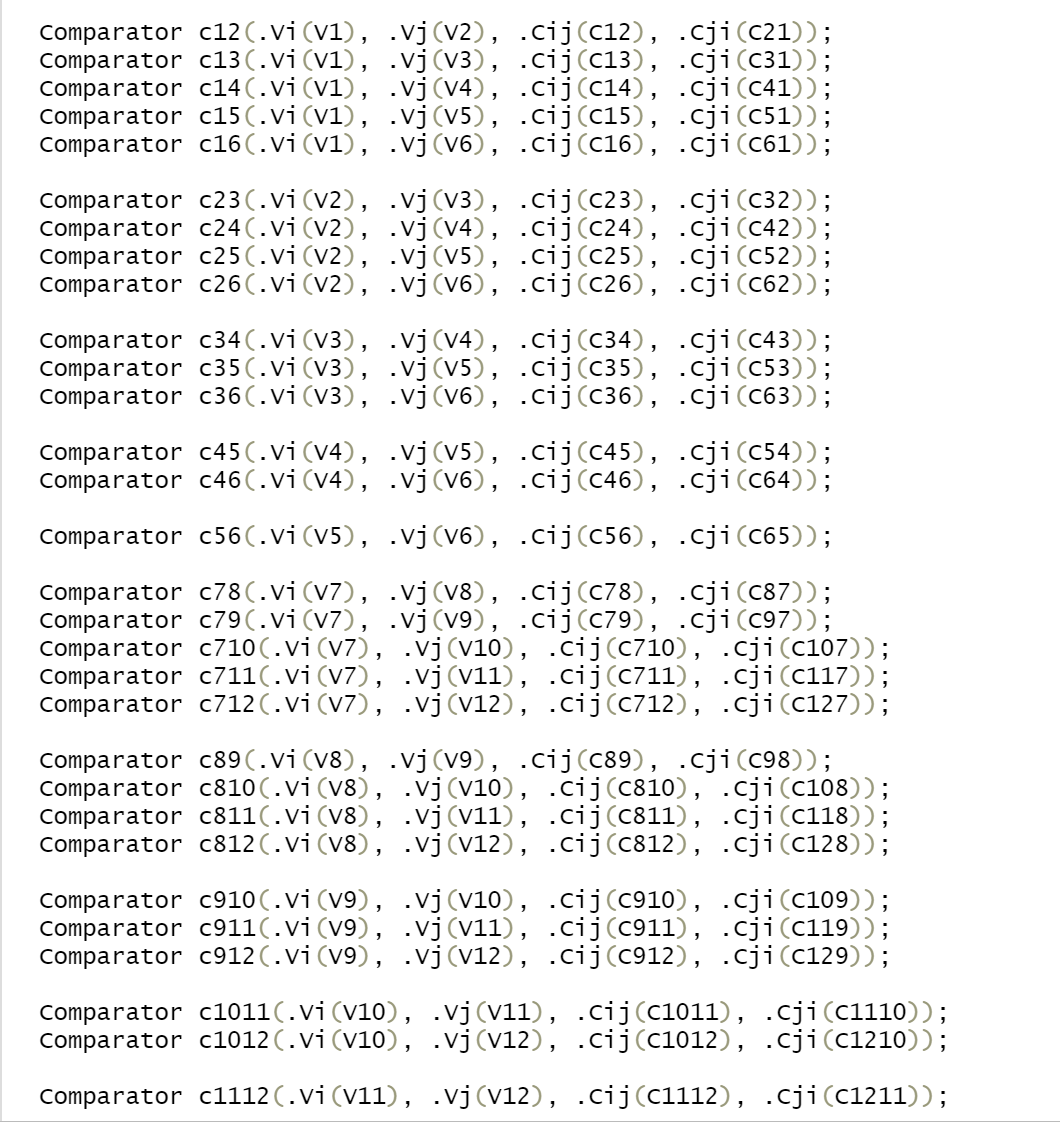
n is the number of capacitors to be turned ON in the upper branch which is input given by the Phase shifted carrier Pulse Width Modulation wave.

Each digit of M represents if the respective capacitor is ON or Bypassed . MSB of M represents status of 6th capacitor in lower branch and LSB of M represents the status of 1st capacitor in upper branch.

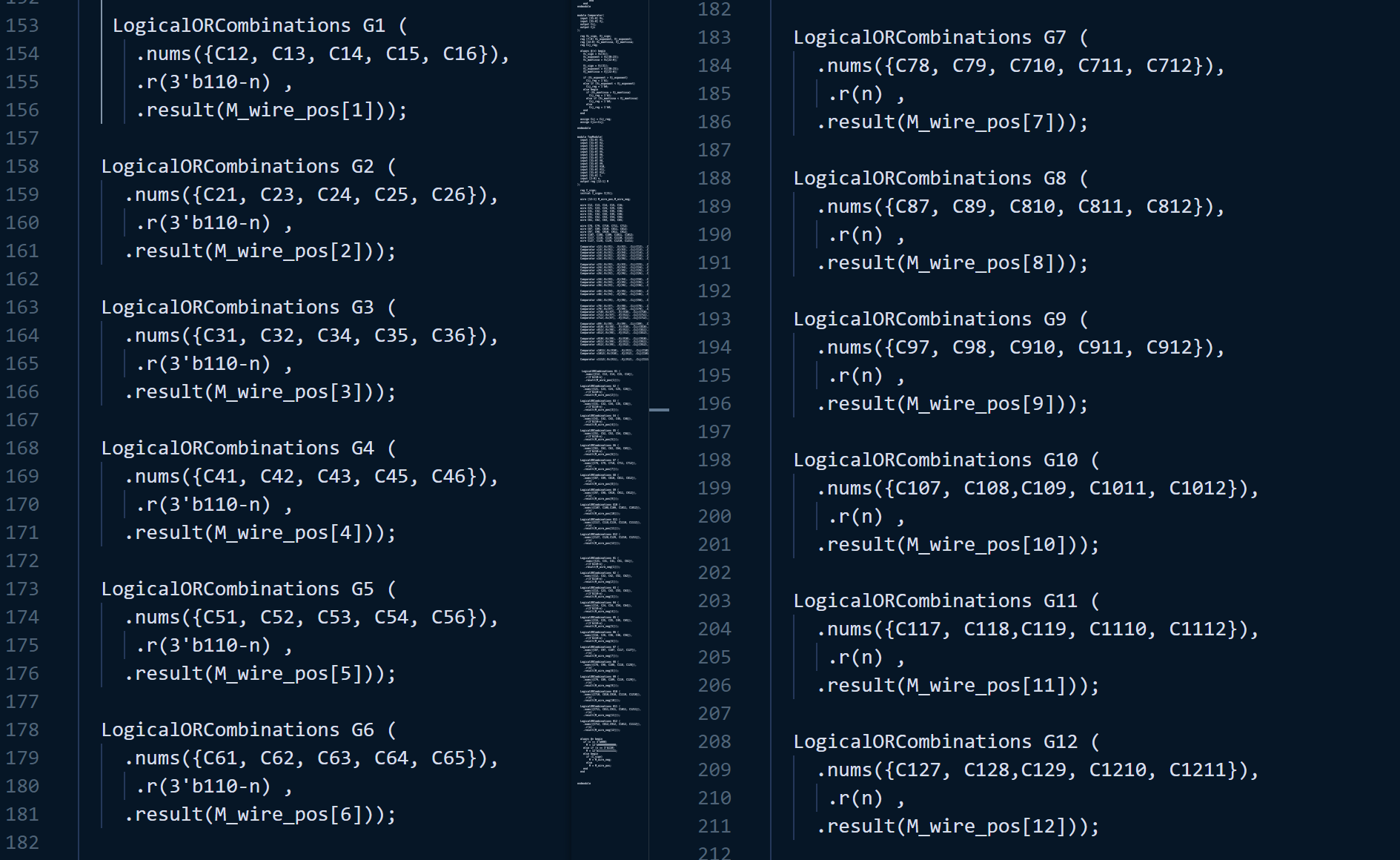
Approach

Instantiating the Comparator module , all possible values of Cij and Cji are obtained.

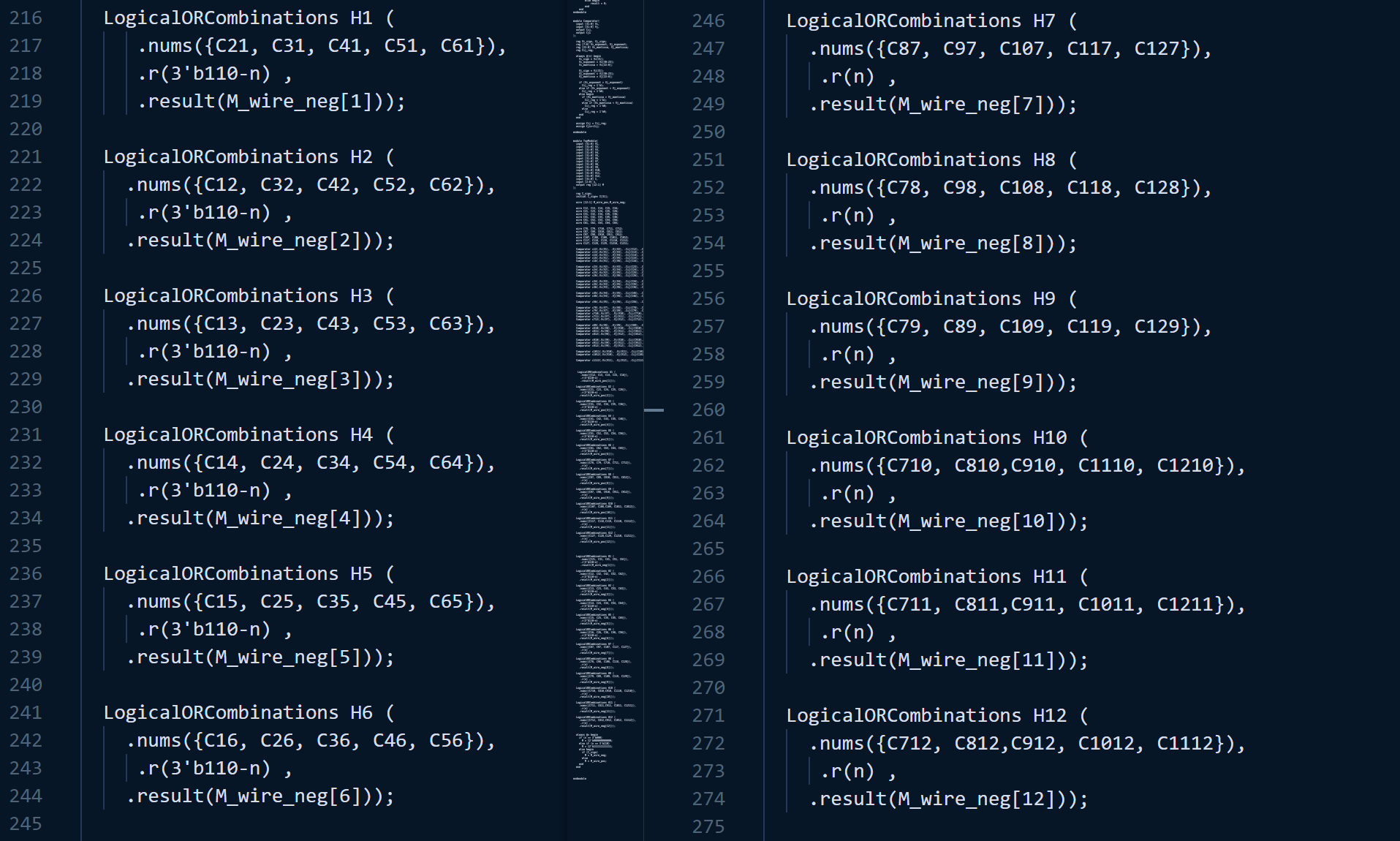
Now since the status of any capacitor is function of Cij’s, so by instantiating the LogicalORCombination Module 12 times, the status of all 12 capacitors are known.



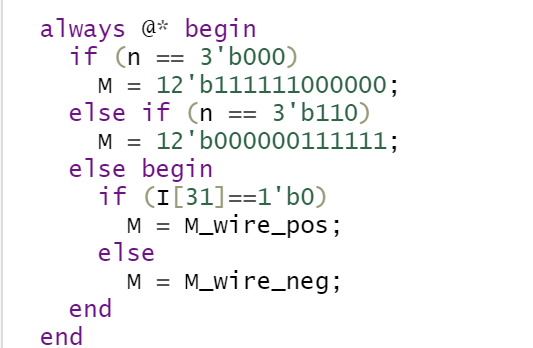
Generating all possible values of Cij’s



Generating output for positive currents

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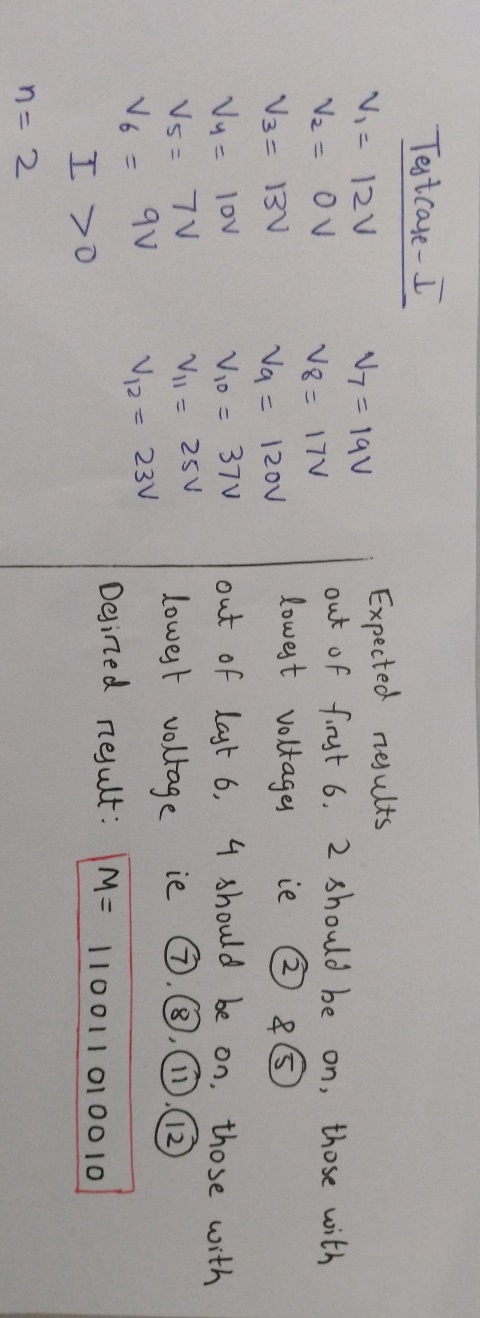
Generating output for negative currents

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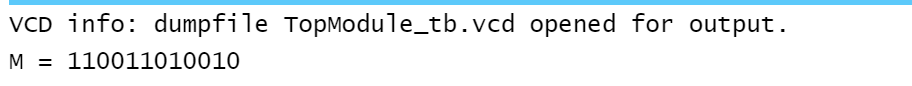
**Assigning final output based of sign of current and input ‘n’**

**Observations**

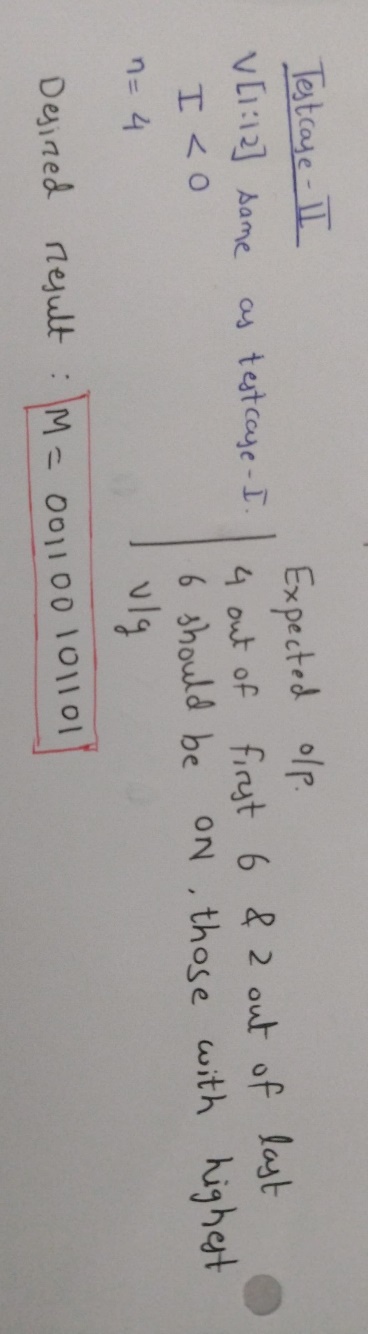
**TestCase-1**

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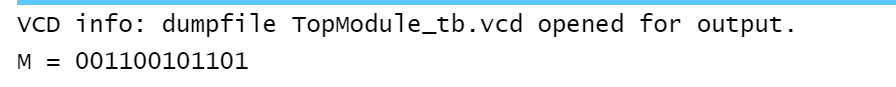
**Output**

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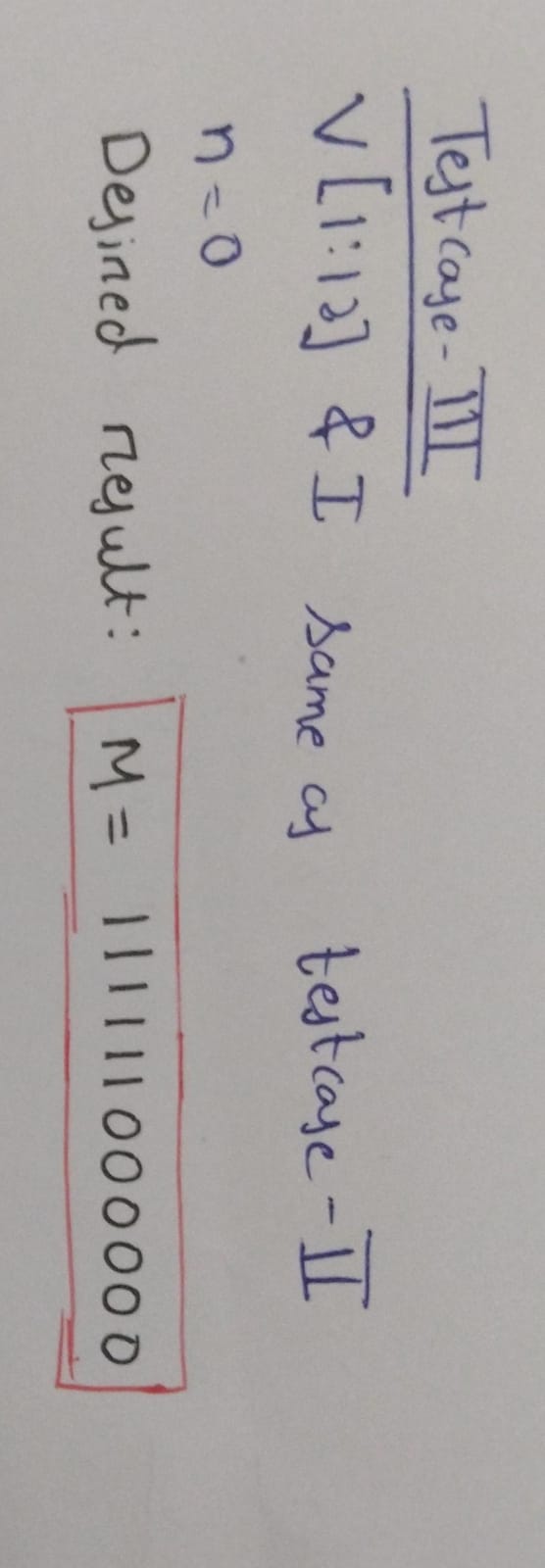
**TestCase-2**

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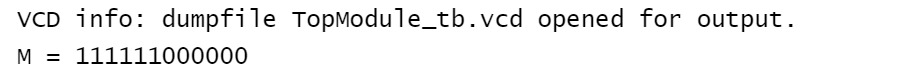
**Output**

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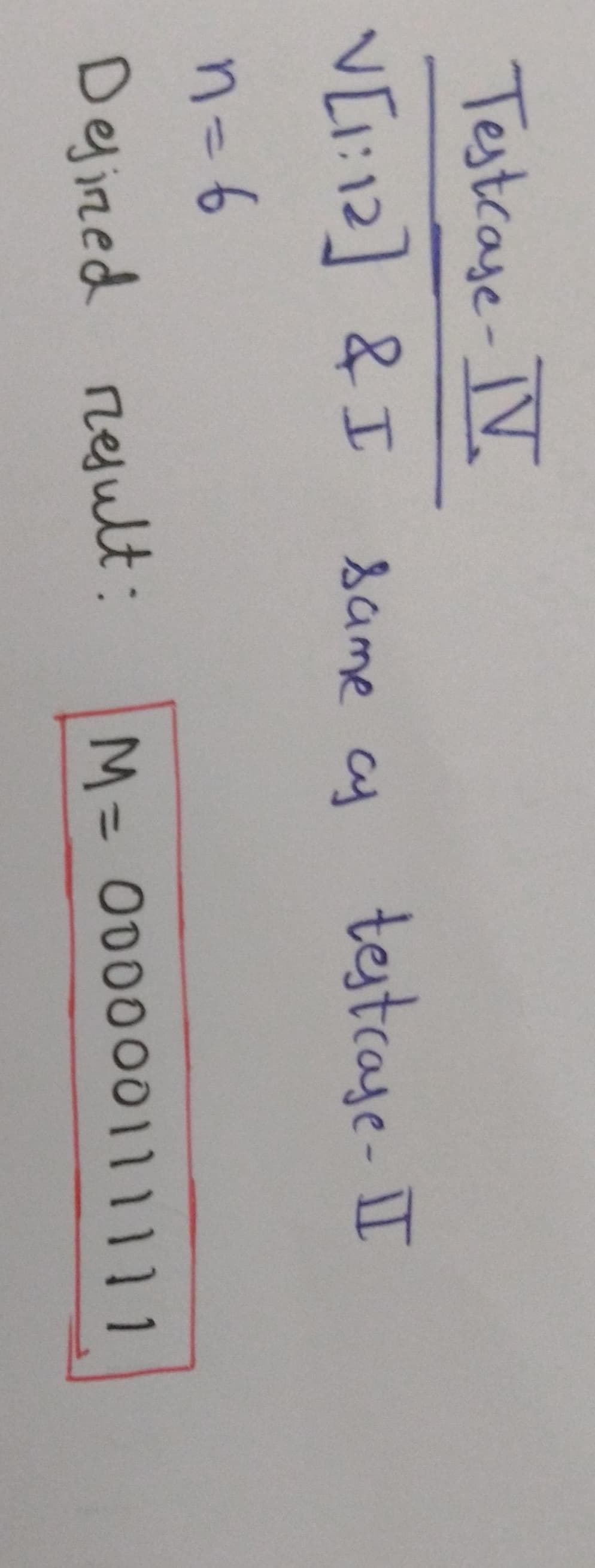
**TestCase-3**

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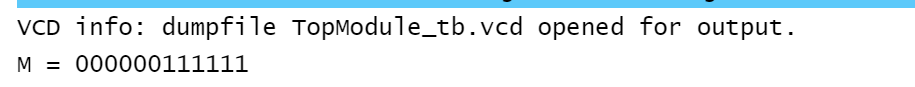
**Output**

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**TestCase-4**

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**Output**

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